



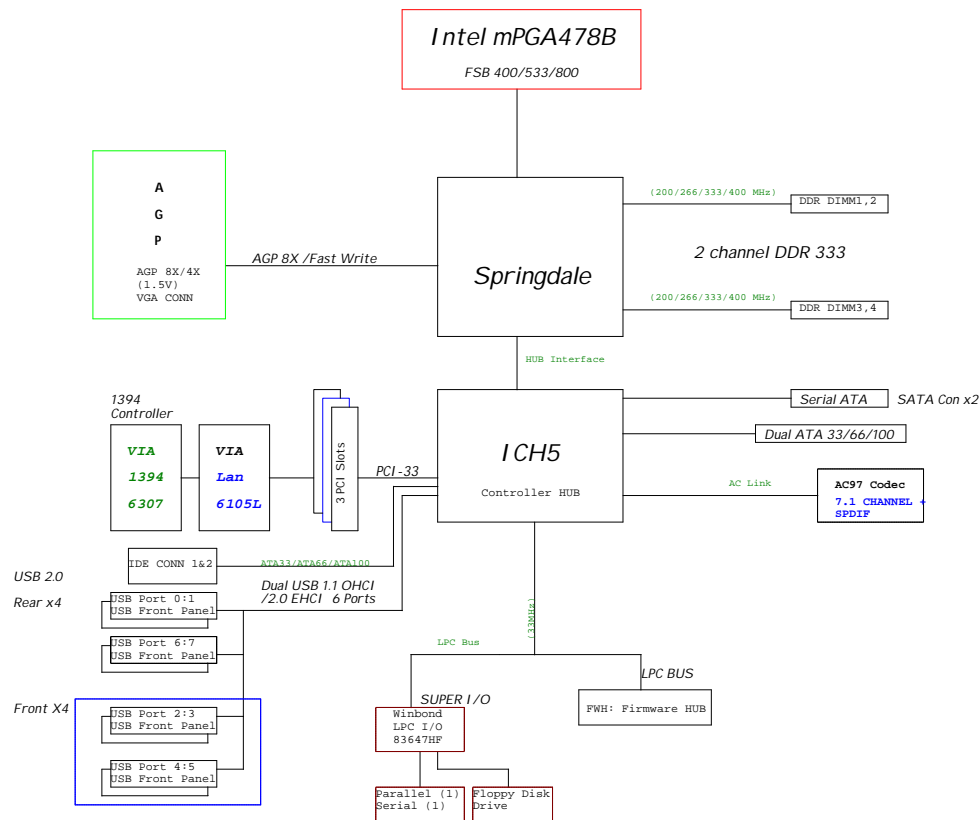
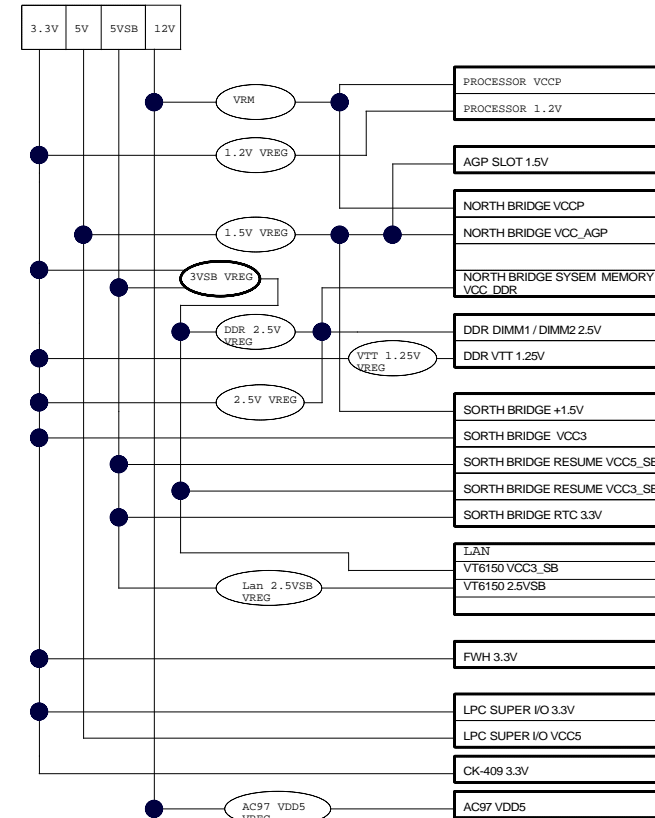
- *INTEL mPGA 478B Processor**
- *INTEL Springdale GMCH / ICH5 Chipset**
(DDR 333 / AGP 8X) / (integrated serial ATA)
- *VIA/6105L**
- *VIA/6306,IEEE1394 3port**
- *Winbond 83637HF LPC I/O**
- *Audio codec 7.16 channel support**
- *USB 2.0 support x8 (integrated into ICH5)**

[illegible]

Block Diagram

+5V : VCC5
 +3.3V : VCC3
 +12V : +12V
 5VSB : VCC5_SB
 -12V : -12V
 +2.55V for DDR : VCC_DDR
 1.275V for DDR VTT : VTT_DDR
 Dual 3.3V : 3VDUAL
 1.2V for CPU VID : VCC_VID
 1.5V for AGP VI/O : VCC_AGP
 Dual 5V : 5VDUAL
 CPU Vcore : VCCP
 +5V for analog CODEC : AVDD5
 2.5V for LAN : 2_5VSB
 +12V for 1394 bus power : CPWR

POWER DELIVERY MAP



GPIO FUNCTION

ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#B	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	GPI8	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	SIO_SMI#	RESUME
GPIO 12	I	EXTSMI#	RESUME
GPIO 13	I	SIO_PME#	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	BIOS_WP#	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	GPO23	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	GPIO25	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	GPIO33	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPUPWRGD	MAIN

default output
default output
default output
default output
default output
default output

FWH

GPIO Pin	Type	Function
GPI 0	I	PD_DET
GPI 1	I	SD_DET
GPI 2	I	BOM strapping for Bit 0
GPI 3	I	Pull down through 1K ohms (unused)
GPI 4	I	BOM strapping for Bit 1

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 2	1010001B	MCLK_A3/MCLK_A3# MCLK_A4/MCLK_A4# MCLK_A5/MCLK_A5#

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 3	1010010B	MCLK_B0/MCLK_B0# MCLK_B1/MCLK_B1# MCLK_B2/MCLK_B2#
DIMM 4	1010011B	MCLK_B3/MCLK_B3# MCLK_B4/MCLK_B4# MCLK_B5/MCLK_B5#

PCI RESET DEVICE

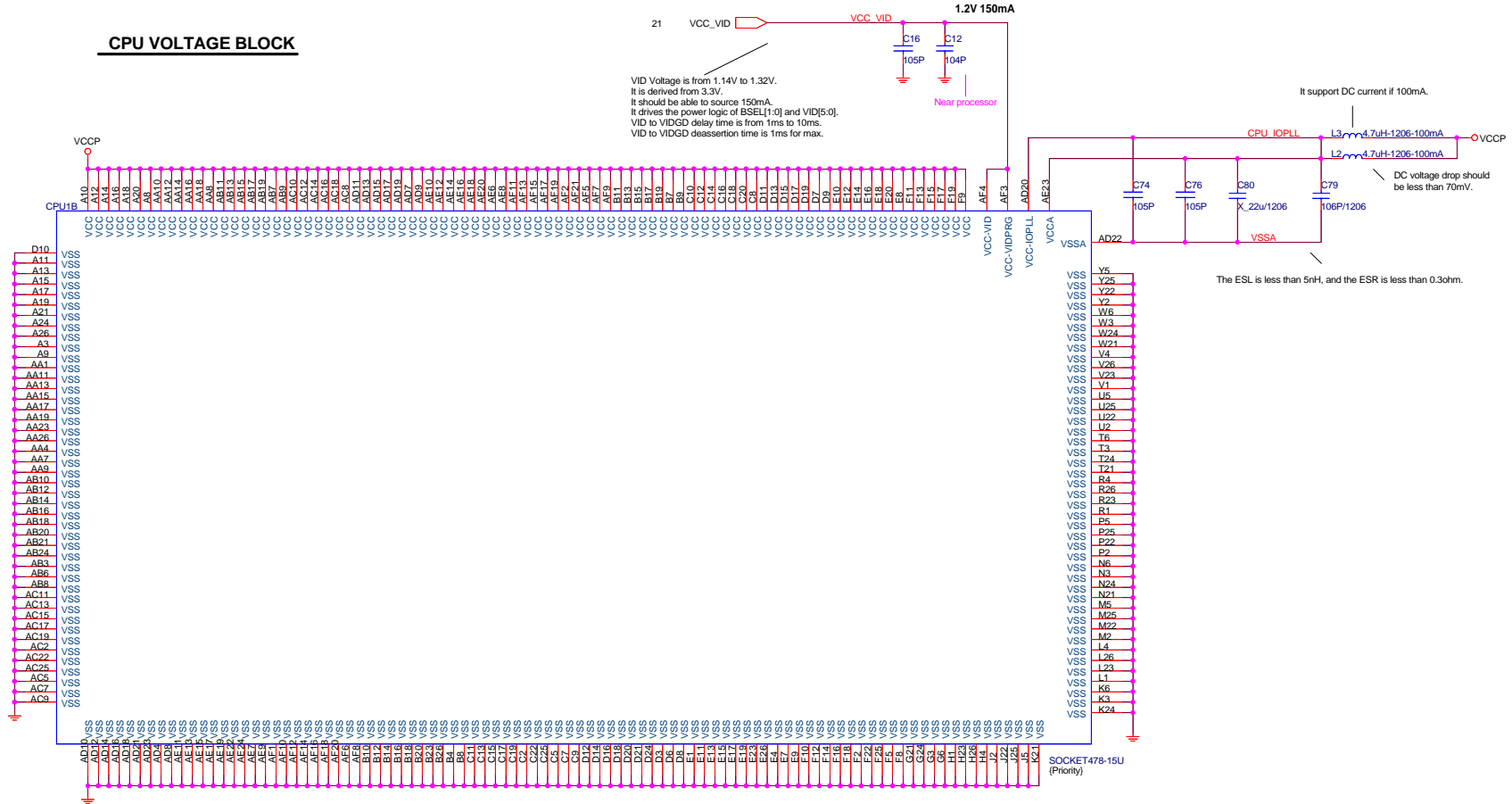
Signals	Target
PCIRST#_ICH5	AGP,FWH,MS-5
PCIRST#1	Springdale,LAN, Super I/O,1394,MS-1
PCIRST#2	PCI slot 1-3 & Mini PCI
HD_RST#	Primary, Scondary IDE

PCI Clock NC pin : PCI 33MHz(Pin 19 ,20) , 66MHz(Pin 27)

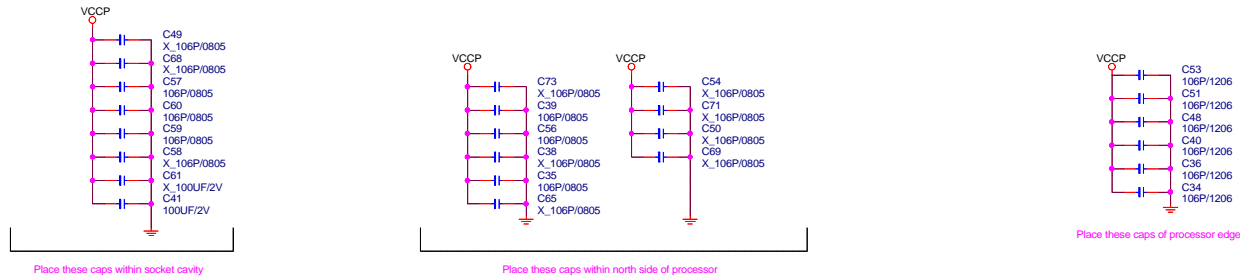
DEVICES	INT#	IDSEL	REQ#/GNT#	CLOCK
Mini PCI 1	INT#A INT#B	AD16	PREQ#1 PGNT#1	PCICLK1-Pin-14
PCI SLOT 1	INT#B INT#C INT#D INT#A	AD17	PCI1PREQ#1 PCI1PGNT#1	PCICLK2-Pin-15
PCI SLOT 2	INT#C INT#D INT#A INT#B	AD18	PREQ#3 PGNT#3	PCICLK3-Pin-20
PCI SLOT 3	INT#D INT#A INT#B INT#C	AD19	PCI3PREQ#3 PCI3PGNT#3	MS1 (MS1PCLK-Pin-8)
PCI SLOT 4	INT#G	AD20	PREQ#5 PGNT#5	PCICLK5-Pin-21
Lan 6105L	INT#E	AD25	PREQ#4 PGNT#4	Lan_PCLK-Pin-16
1394	INT#F	AD26	PREQ#2 PGNT#2	1394_PCLK-Pin-12
MS-1			PREQ#0 PGNT#0	MS1PCLK-Pin-8

Micro Star Restricted Secret			
Title		GPIO Spec.	
Document Number		MS-7048	
MICRO-STAR INT'L No. 66, No. 1 St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, December 30, 2003 Sheet 3 of 28	

CPU VOLTAGE BLOCK

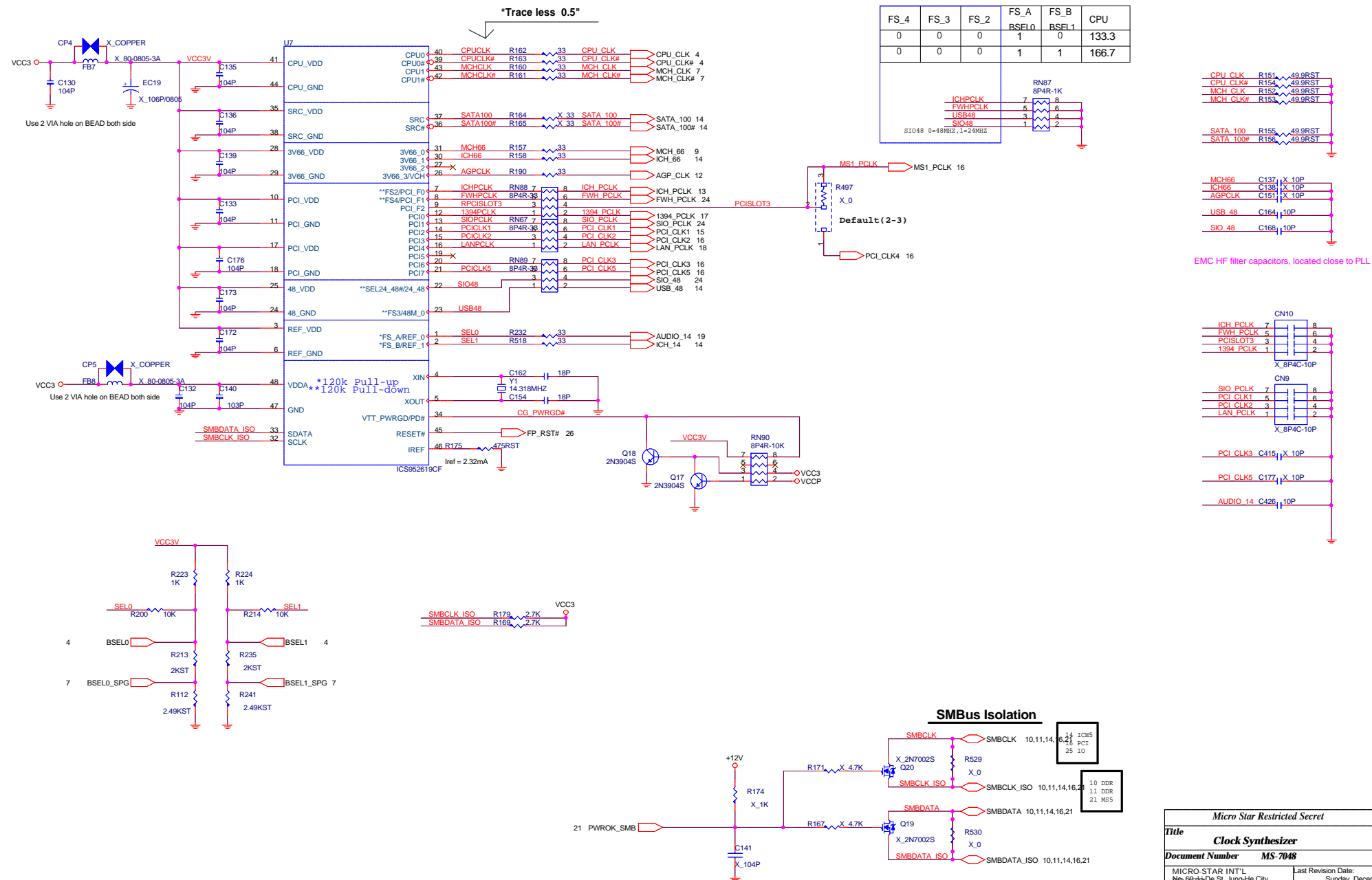


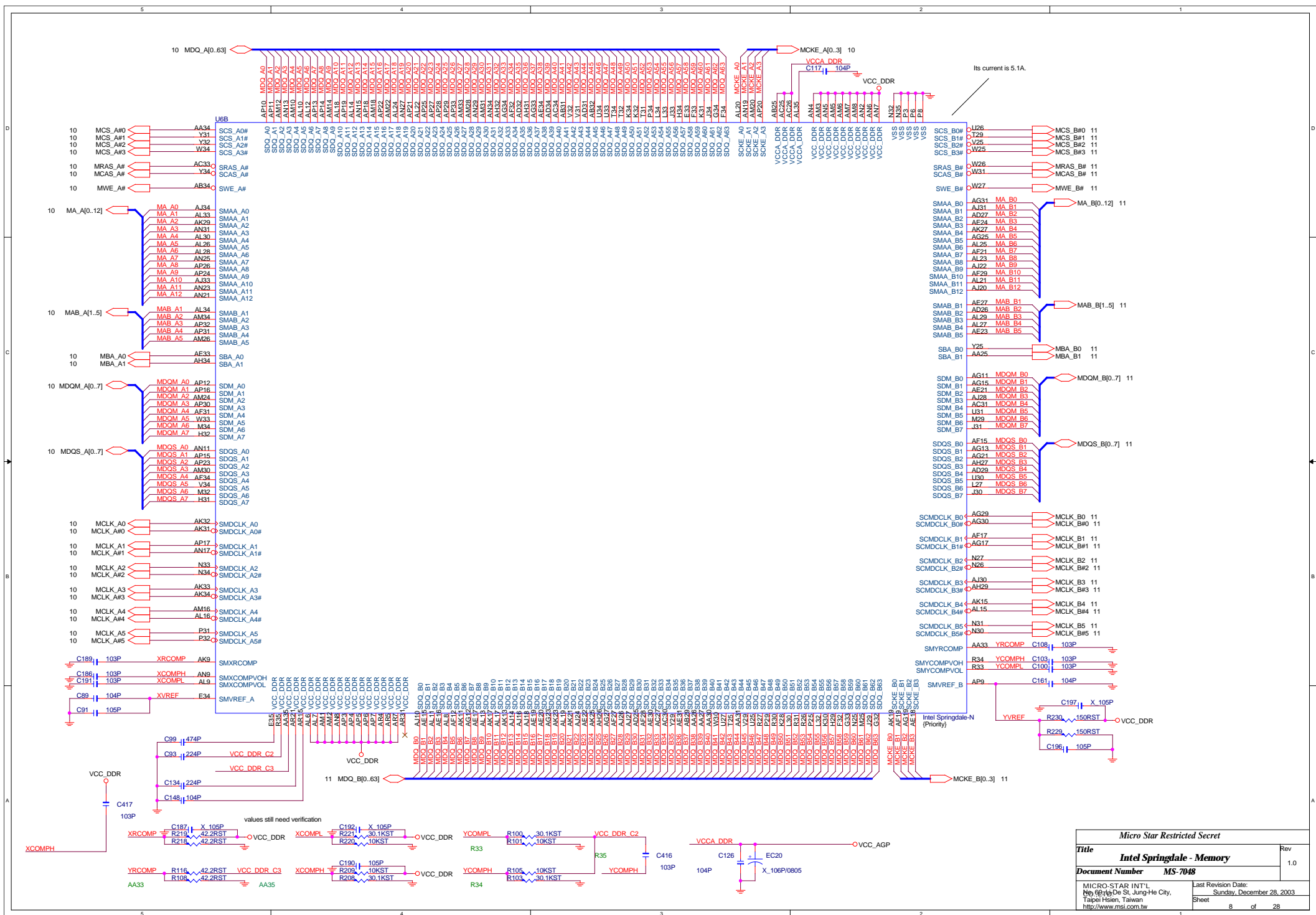
CPU DECOUPLING CAPACITORS

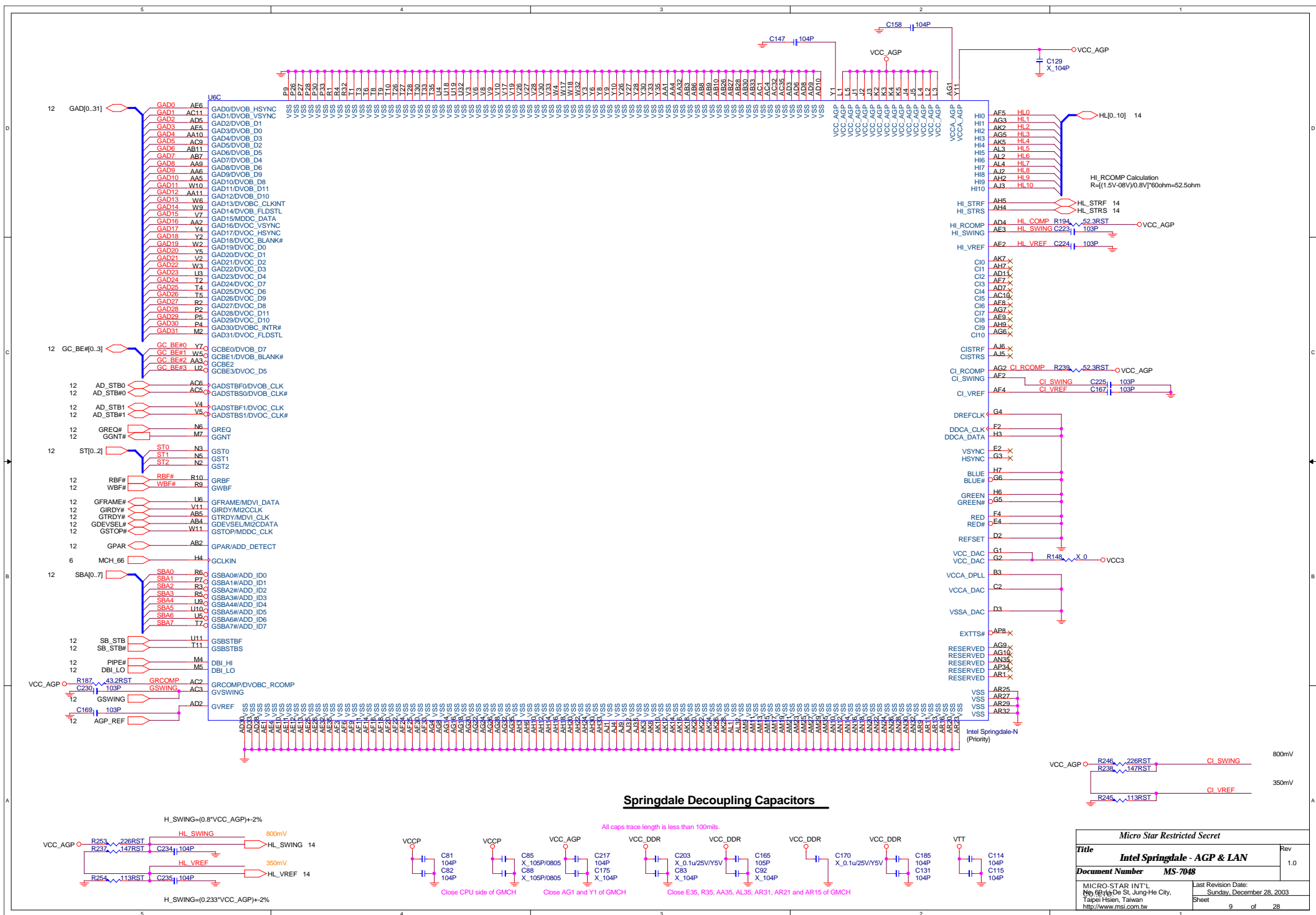


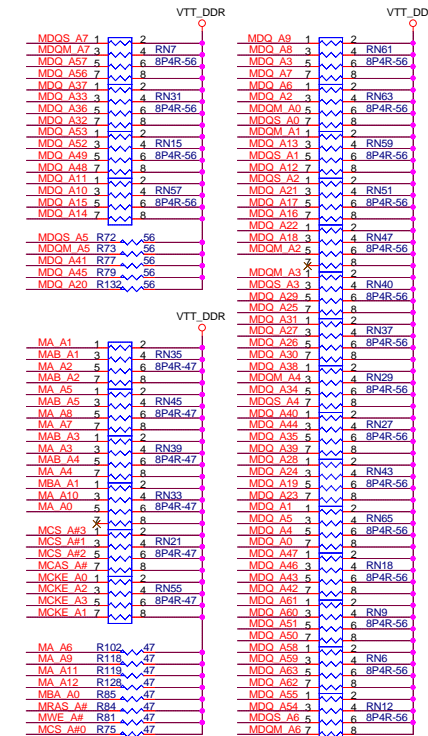
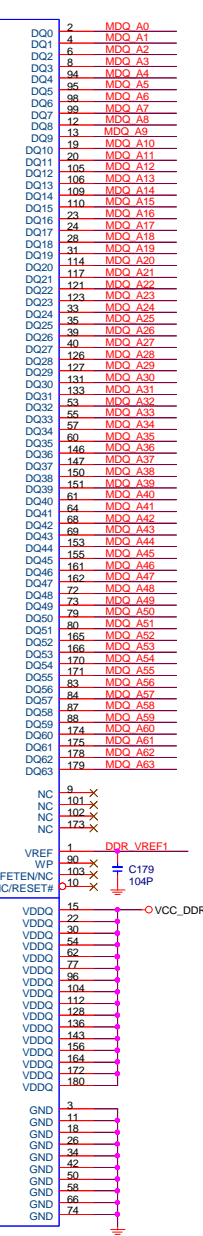
Micro Star Restricted Secret		
Title	Intel mPGA478B - Power	Rev 1.0
Document Number	MS-7048	
MICRO-STAR INT'L No. 66, De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Sunday, December 28, 2003 Sheet 5 of 28

Clock Synthesizer









ADDR.=1010001B

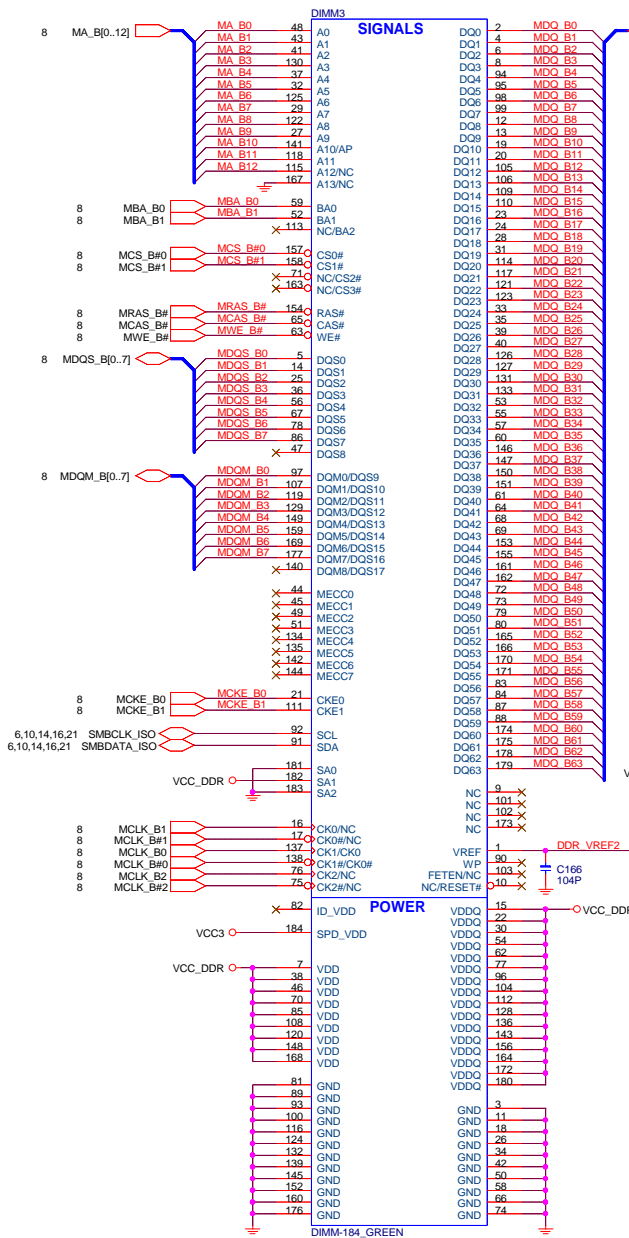
Micro Star Restricted Secret		
Title	DDR DIMM 1,2	Rev 1.0
Document Number	MS-7048	
MICRO-STAR INT'L №Đ 54NgĐe St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Sunday, December 28, 2003 Sheet 10 of 28

SYSTEM MEMORY

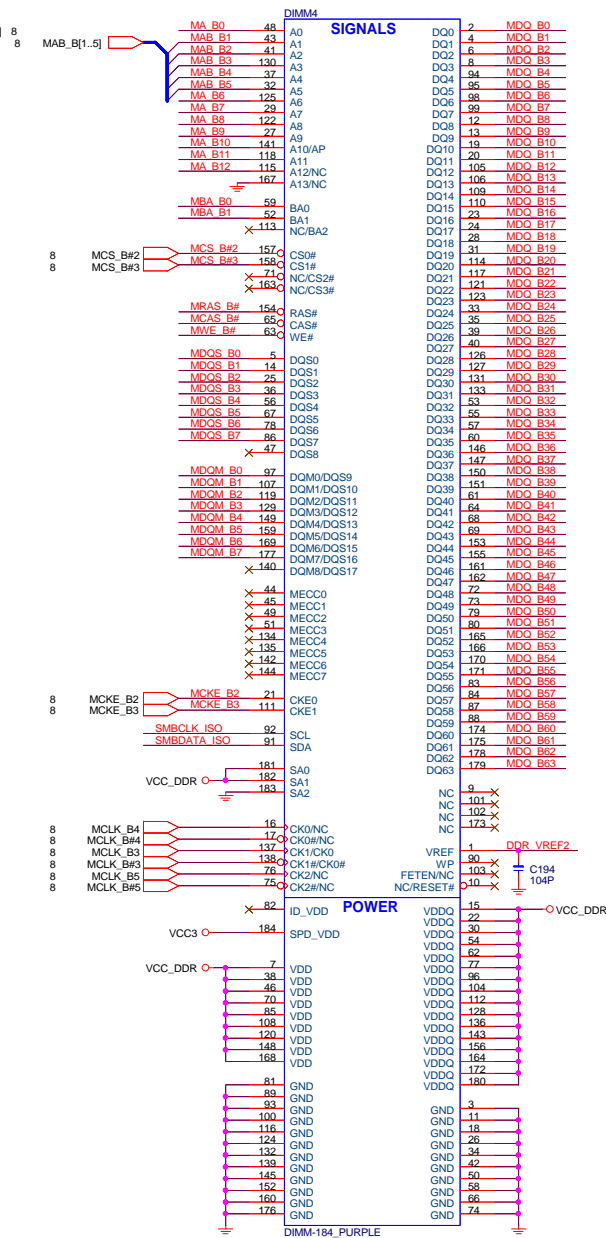
DDR DIMM3

DDR DIMM4

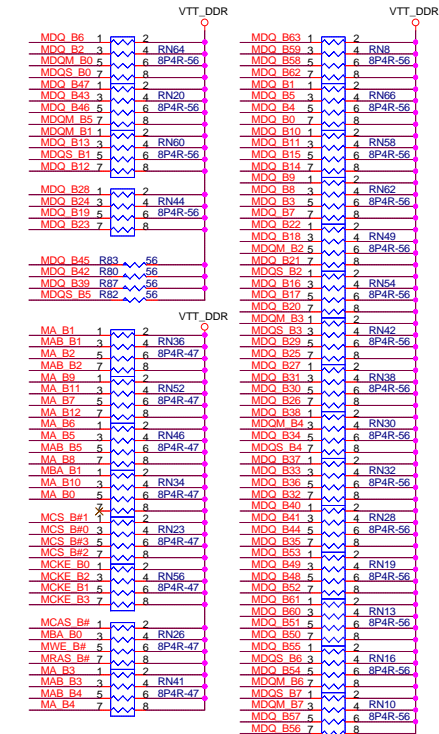
DDR Terminational Resistors



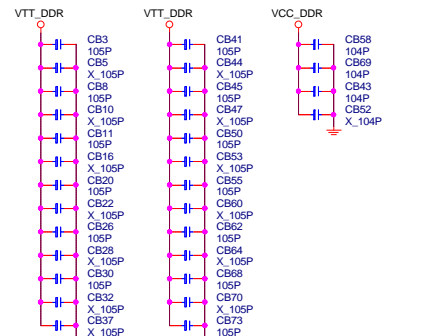
ADDR.=1010010B



ADDR.=1010011B



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

Micro Star Restricted Secret		
Title	DDR DIMM 3.4	Rev
Document Number	MS-7048	1.0
MICRO-STAR INT'L No. 66, De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Sunday, December 28, 2003 Sheet 11 of 28

Medion AGP

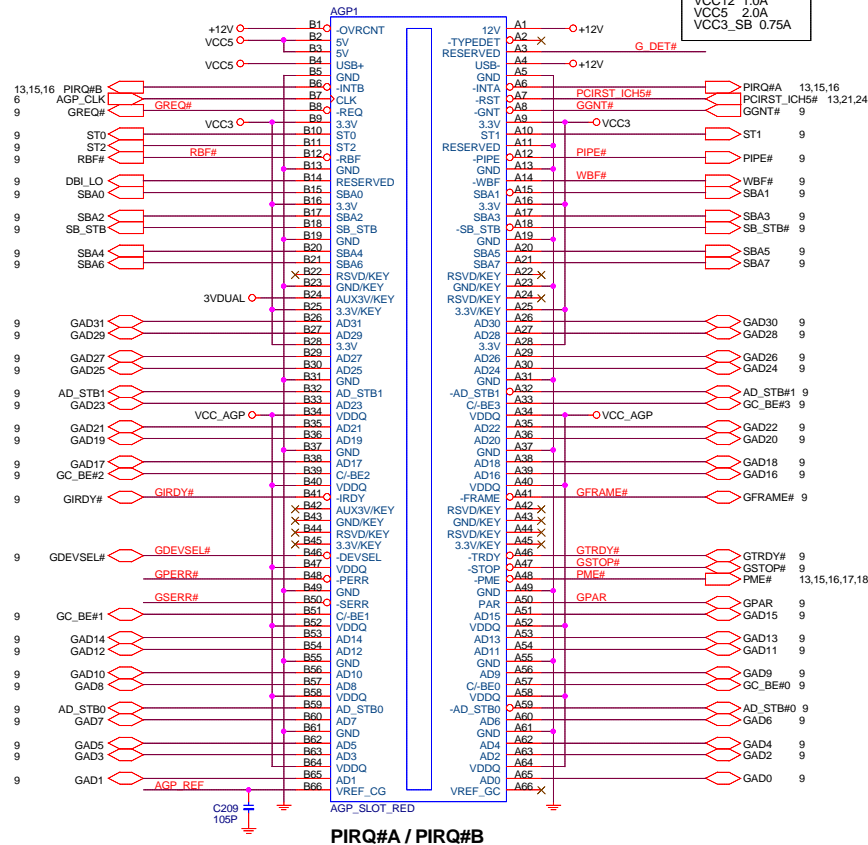
B1 == 12V
A4 == 12V
B4 == 5V

AGP 1.5V 4X/8X SLOT(AGP VER:3.0)

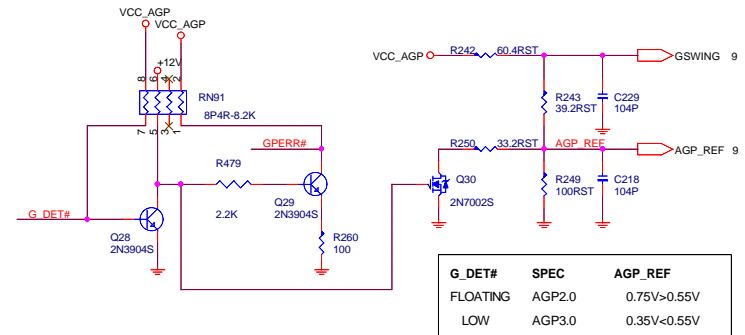
VCC5 = 60mils trace / 15 mils space

AGP Slot Imax

VCCg 2.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A
VCC3_SB 0.75A



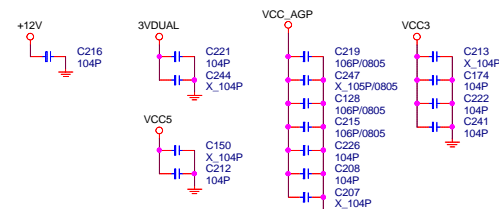
Springdale Reference & Swing Voltage Circuit



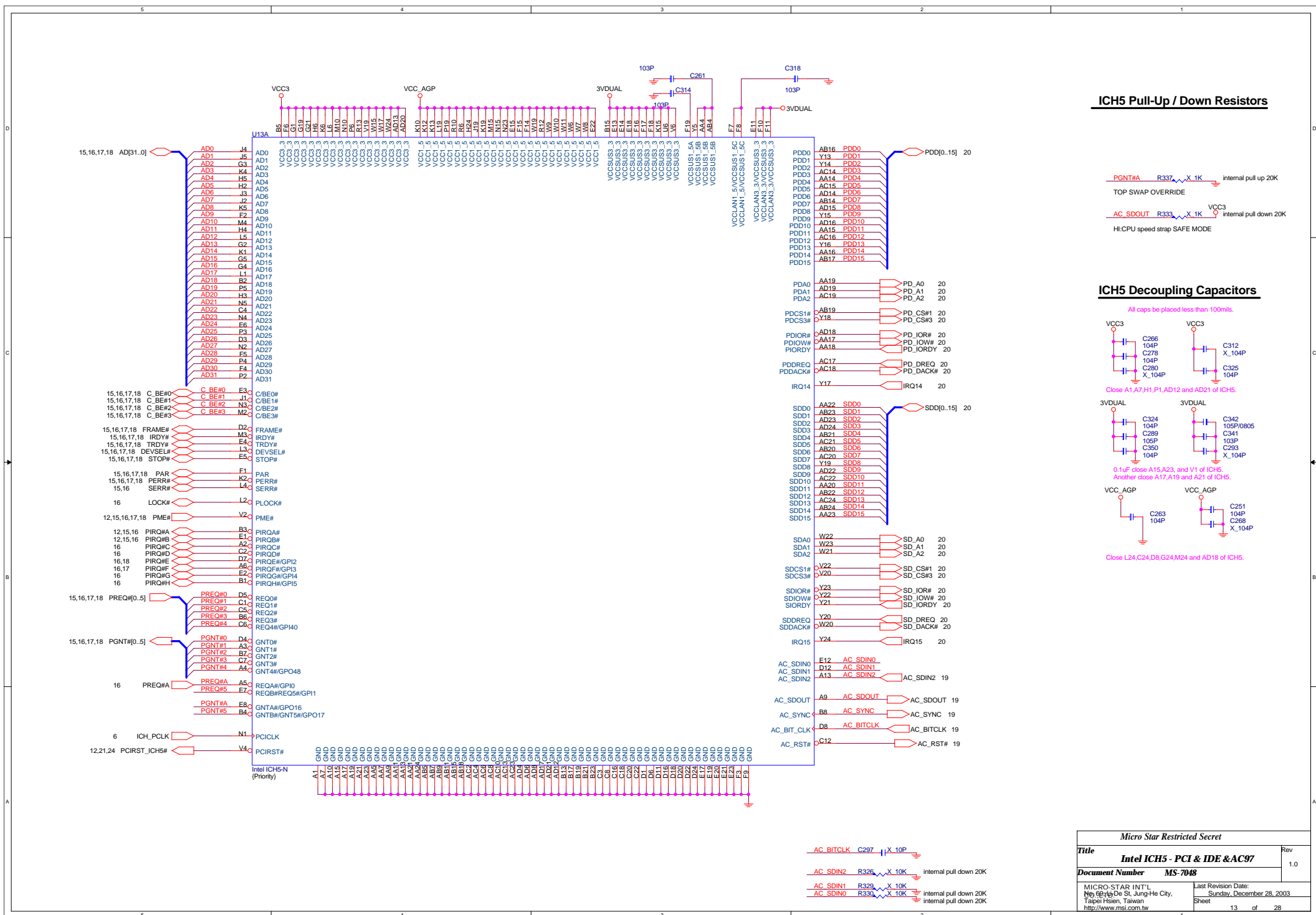
AGP TERMINATION RESISTORS

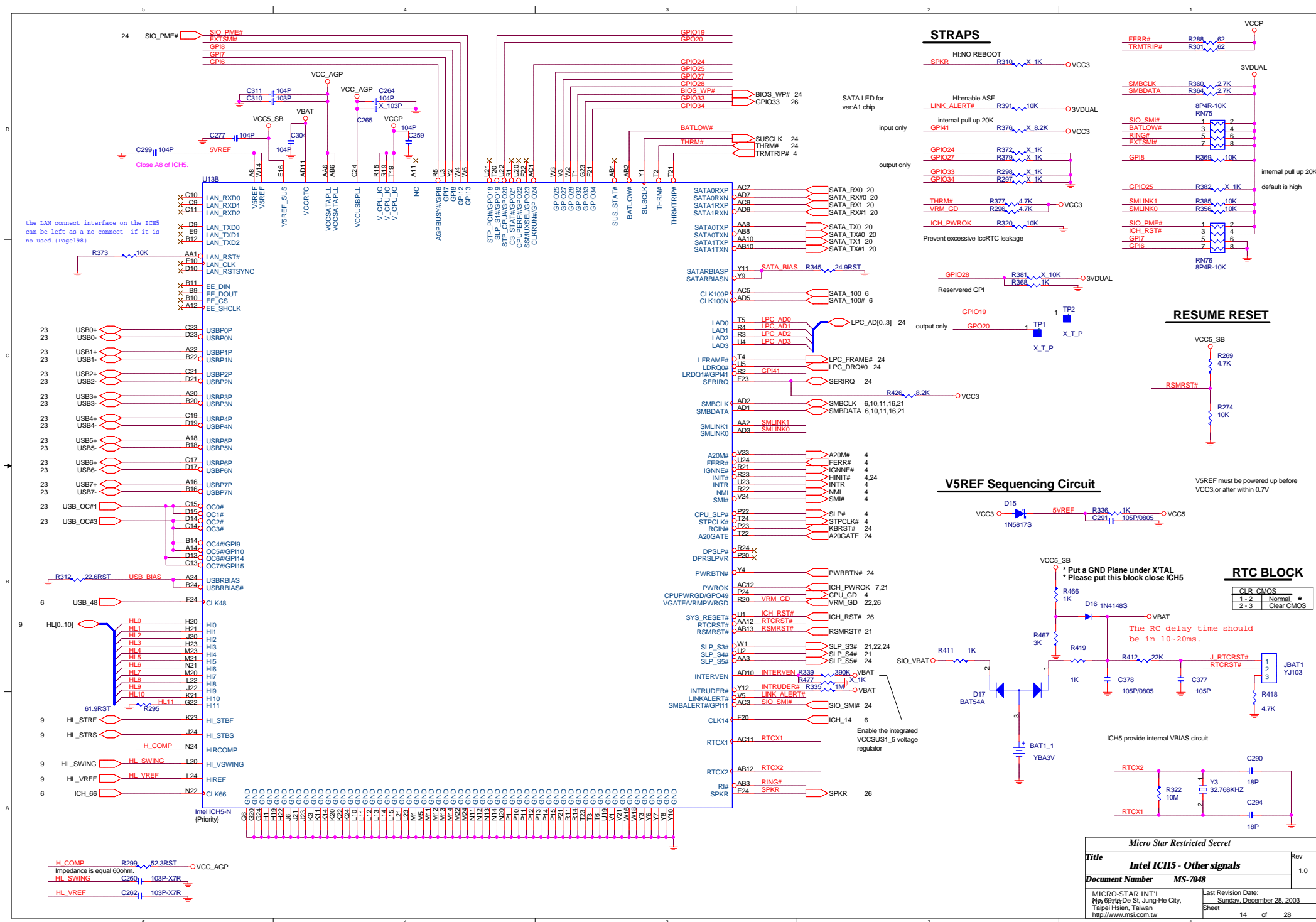


AGP SLOT DECOUPLING CAPACITORS

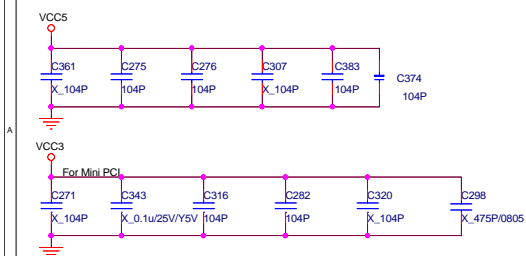
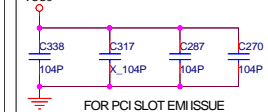
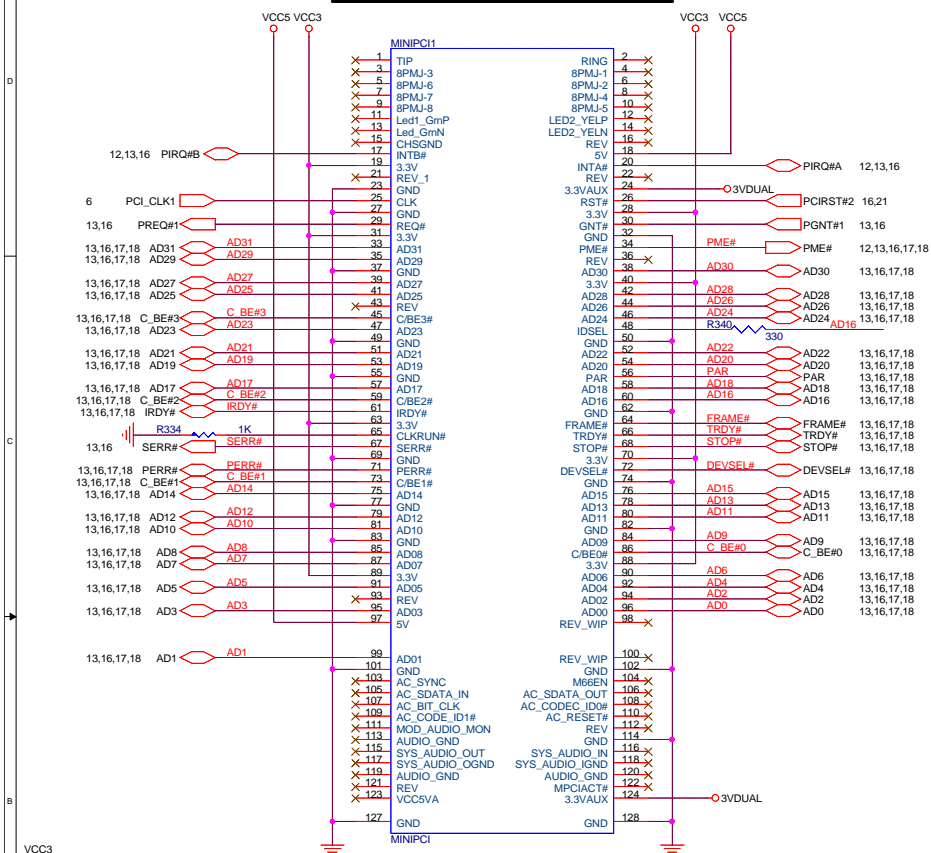


Micro Star Restricted Secret		
Title	AGP SLOT	Rev
Document Number	MS-7048	1.0
Last Revision Date: Sunday, December 28, 2003		
MICRO-STAR INT'L No. 6674 De St. Jung-He City, Taipei Hsien, Taiwan		
http://www.msi.com.tw		
Sheet 12 of 28		

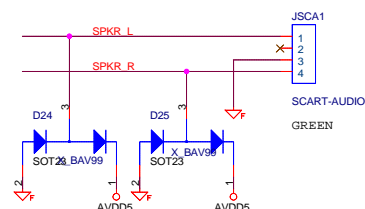




IDSEL = AD16
MASTER = PREQ#1/PGNT#1
PIRQ#A CLK-gen-Pin14
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

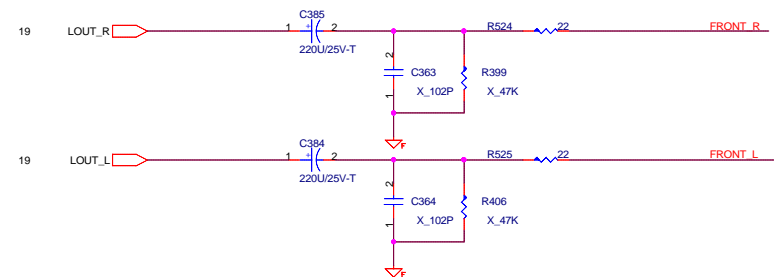


SCART INTERFACE AUDIO OUT



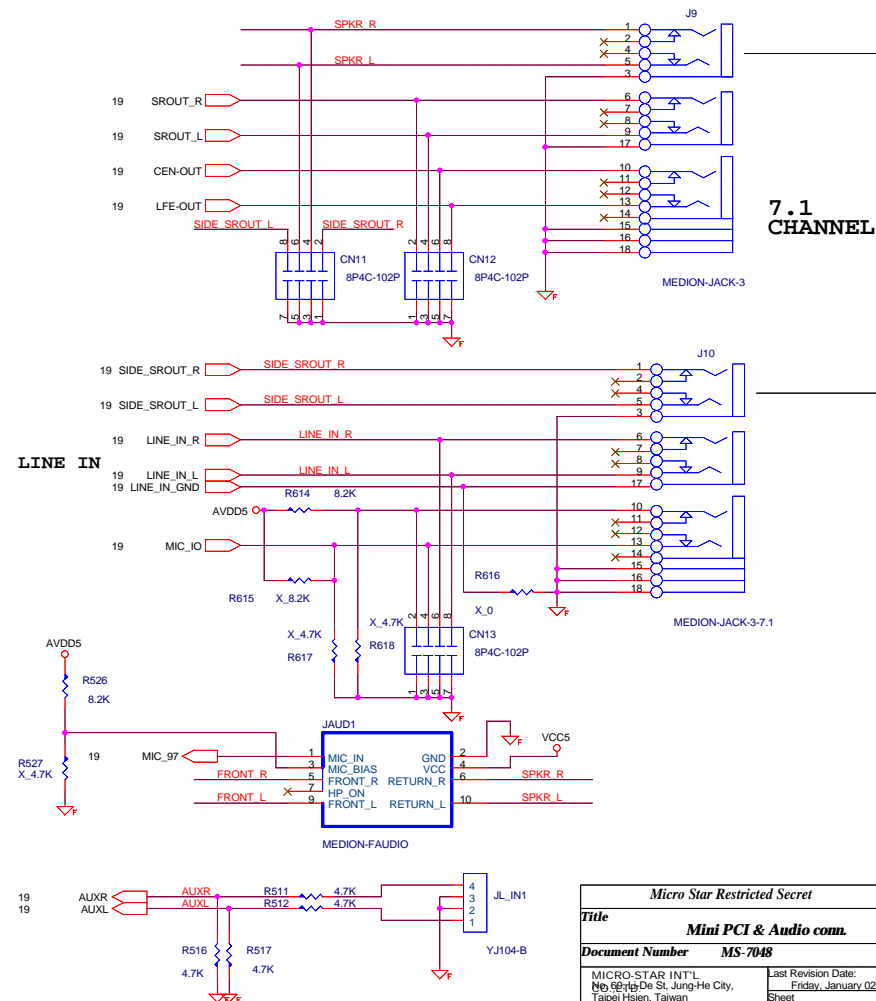
FRONT AUDIO

SPEAKER OUT CIRCUIT



Audio Connector

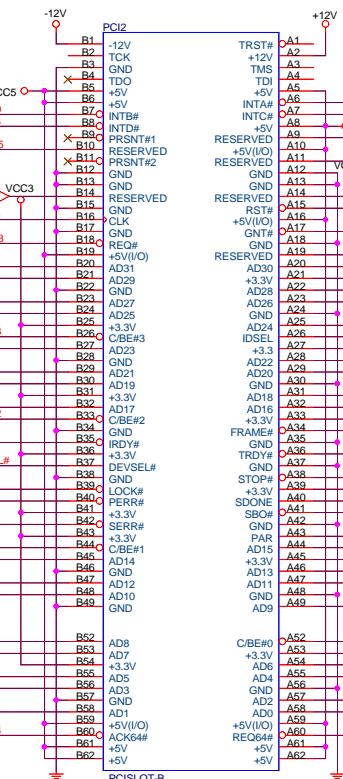
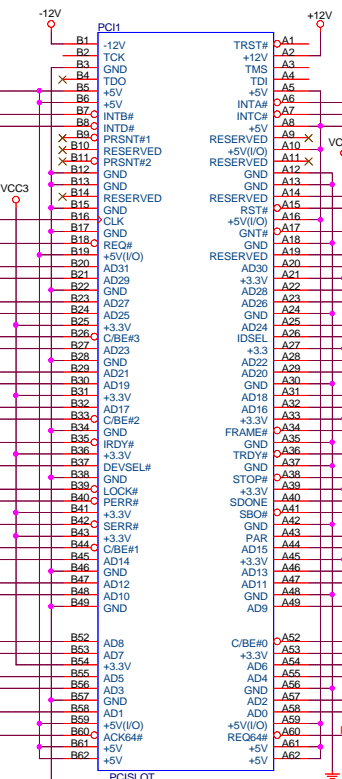
N54-13F0011-K06
CN-IOC-JACKx3+PHONE-D13



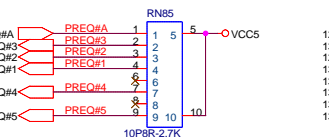
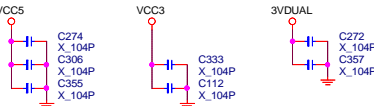
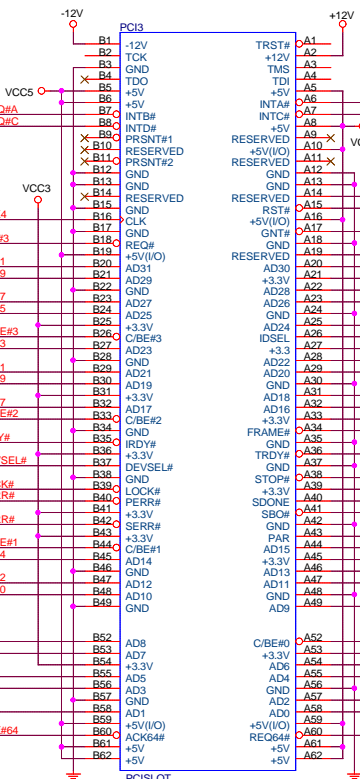
7.1 CHANNEL

LINE IN

Micro Star Restricted Secret			
Title	Mini PCI & Audio conn.		Rev
Document Number	MS-7048		1.0
MICRO-STAR INT'L No. 669, Sec 2, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, January 02, 2004 Sheet 15 of 28	



VCC3
C489
X_102P
EMI, NEAR R343

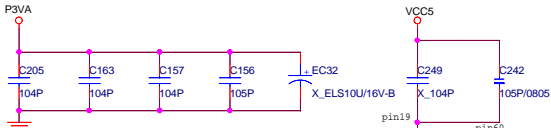


3			Micro Star Restricted Secret		
Title					Rev
PCI Slot 1 & 2 & 3					1.
Document Number					MS-7048
MICRO-STAR INT'L No 99, Sec 2, Jung-Ho City, Taichung Hsien, Taiwan http://www.msi.com.tw					Last Revision Date: Sunday, December 28, 2003 Sheet 16 of 28

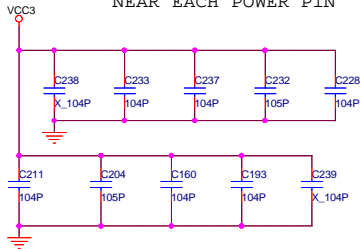
IEEE-1394

INTF# AD26
PREQ#/PGNT#2
Did not support S3
wake-up

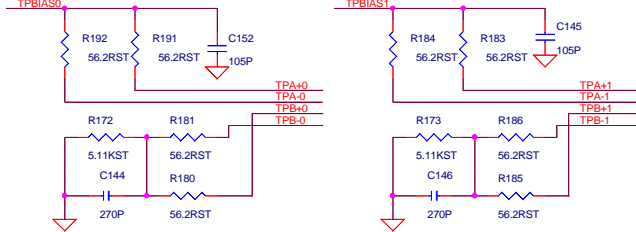
13,15,16,18 AD[31:0]



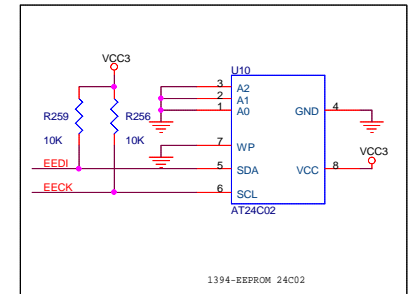
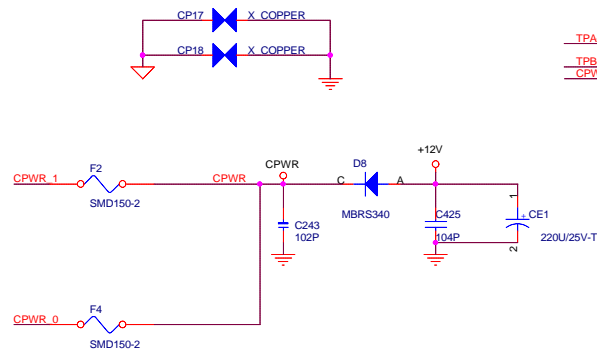
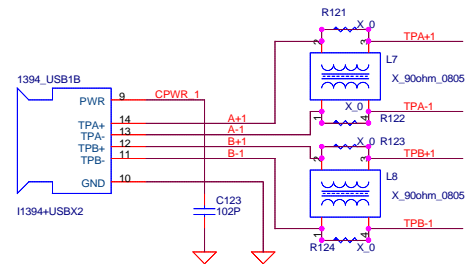
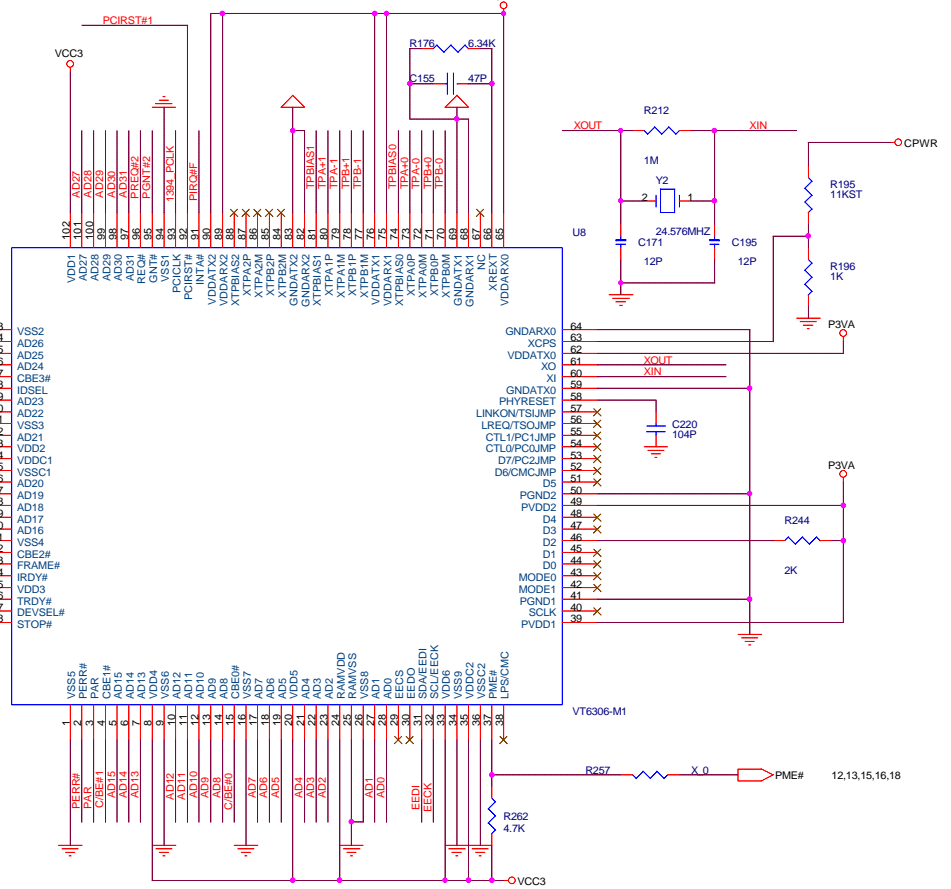
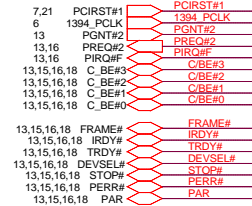
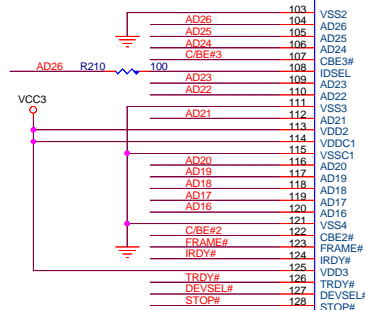
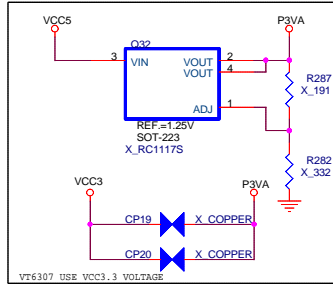
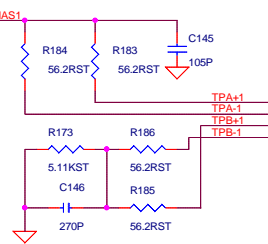
NEAR EACH POWER PIN



Place near chip side

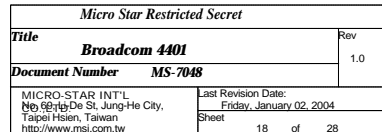


Place near chip side

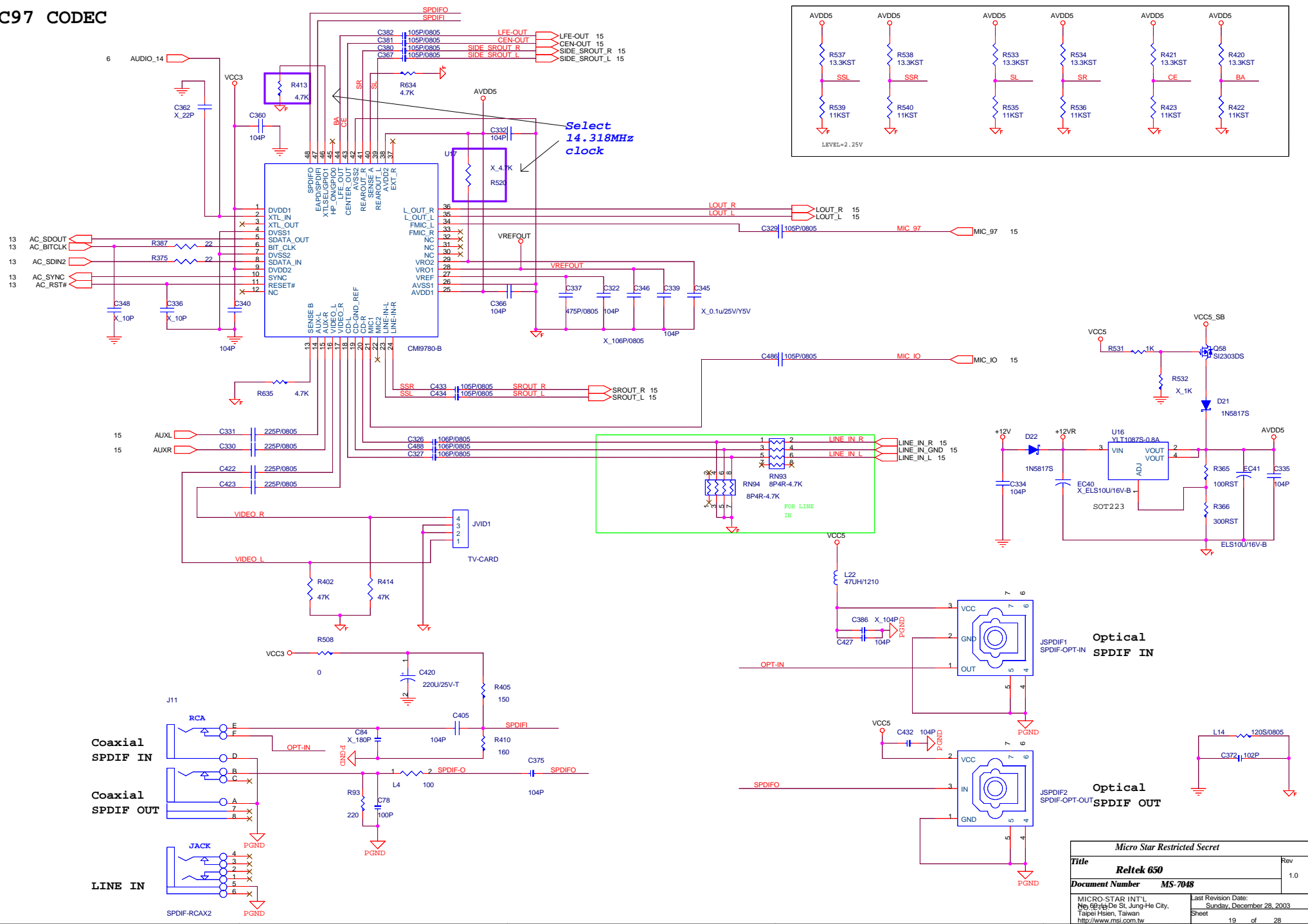


Micro Star Restricted Secret		
Title	IEEE 1394(NEC)	Rev
Document Number	MS-7048	1.0
MICRO-STAR INT'L No. 66, De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, January 02, 2004 Sheet 17 of 28

REQ#/GNT#4
INTE# AD25

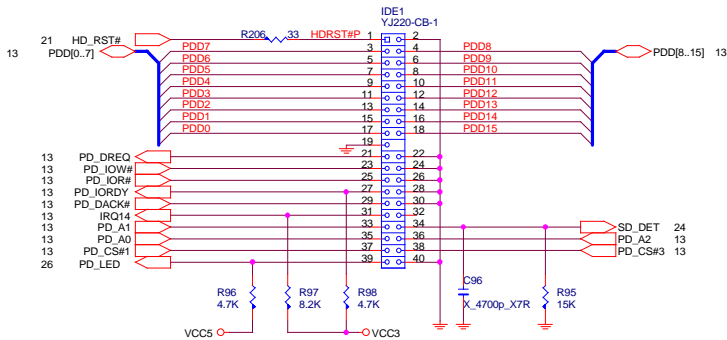


AC97 CODEC

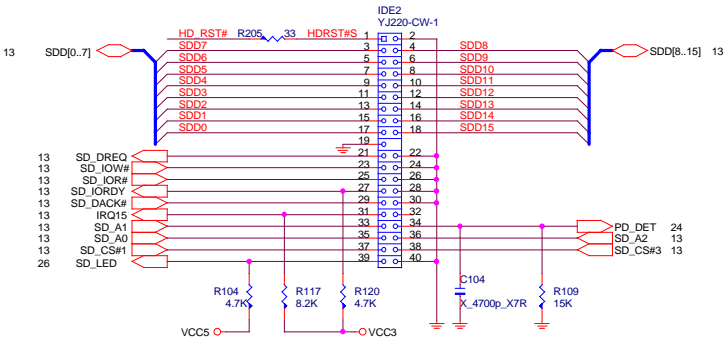


ATA 33/66/100 Connector

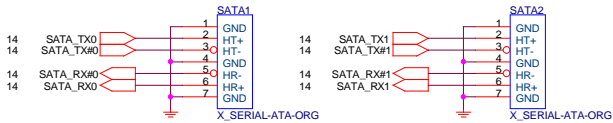
PRIMARY IDE BLOCK



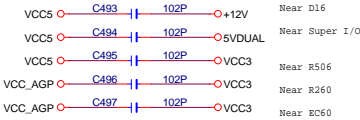
SECONDARY IDE BLOCK



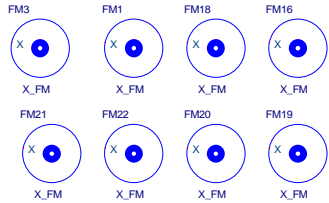
SERIAL ATA CONNECTOR BLOCK



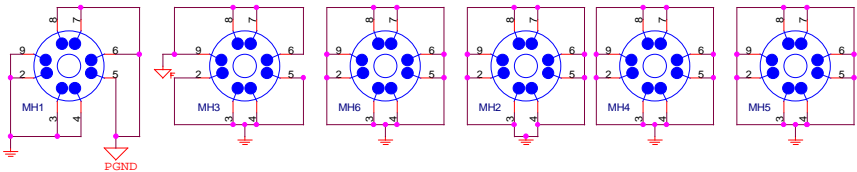
EMI



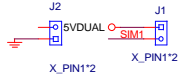
Optics Orientation Holes



Mounting Holes



Simulation



Micro Star Restricted Secret		
Title	ATA 33/66/100 Connector	Rev 1.0
Document Number	MS-7048	
MICRO-STAR INT'L No. 66, Sec. 2, St. Jung-Ho City, Taipen Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Sunday, December 28, 2003 Sheet 20 of 28

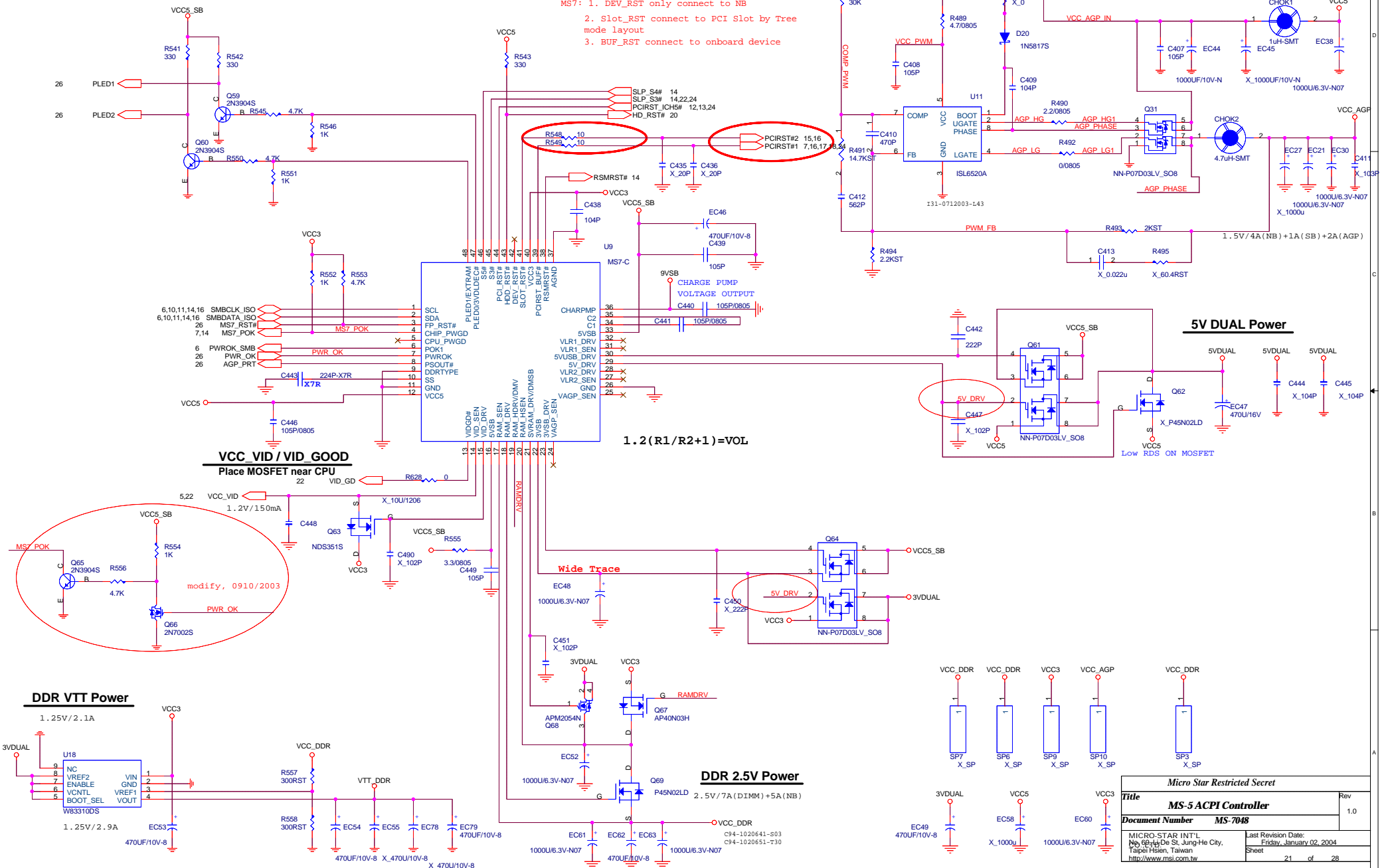
ACPI Controller

	ICH5 300mA
PCI	375+20+20= 415mA
<hr/>	
VCC3_SB	715mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

MS7: 1. DEV_RST only connect to NB
2. Slot_RST connect to PCI Slot by Tree mode layout
3. BUF_RST connect to onboard device

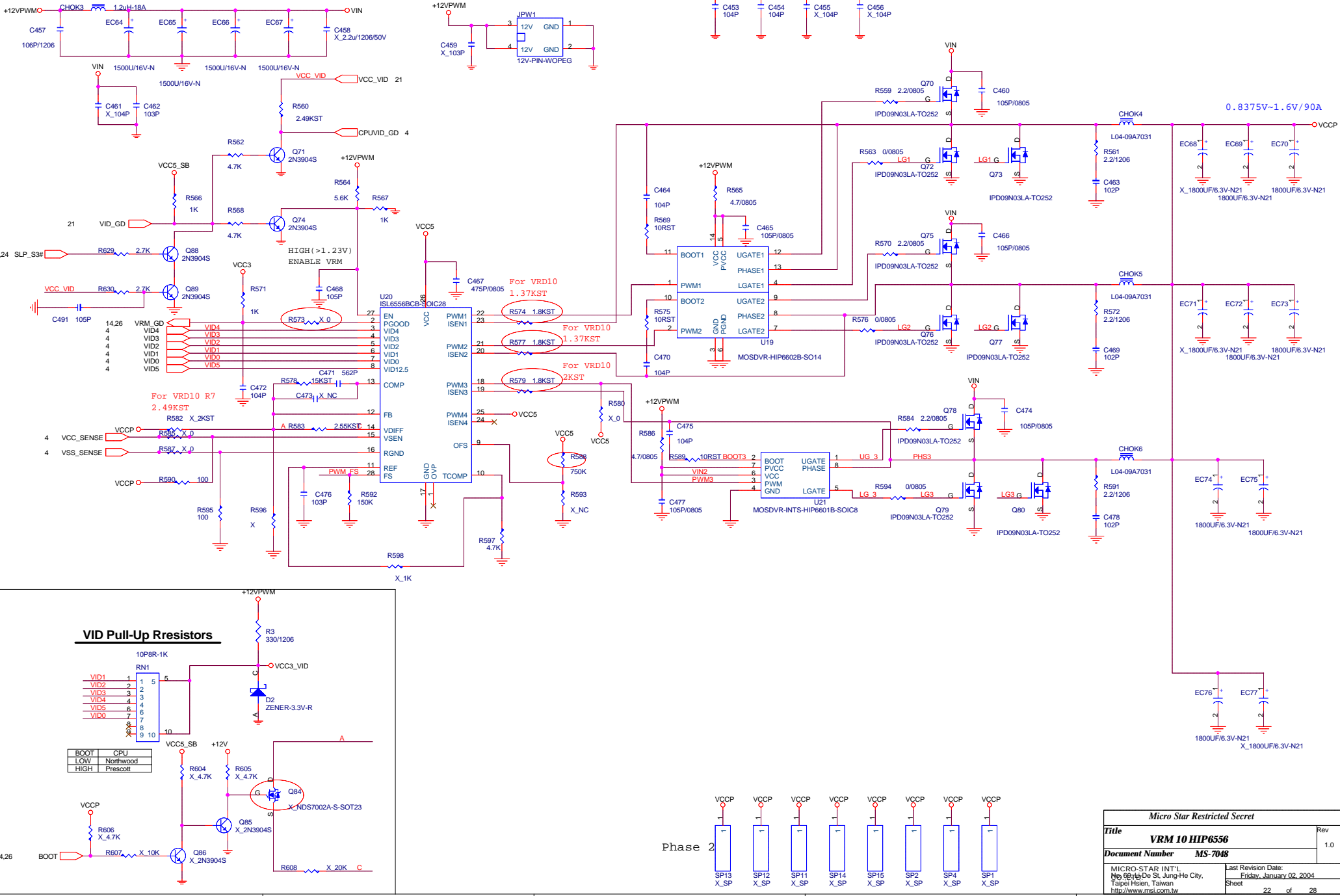
VCC 1.5 Voltage Regulator



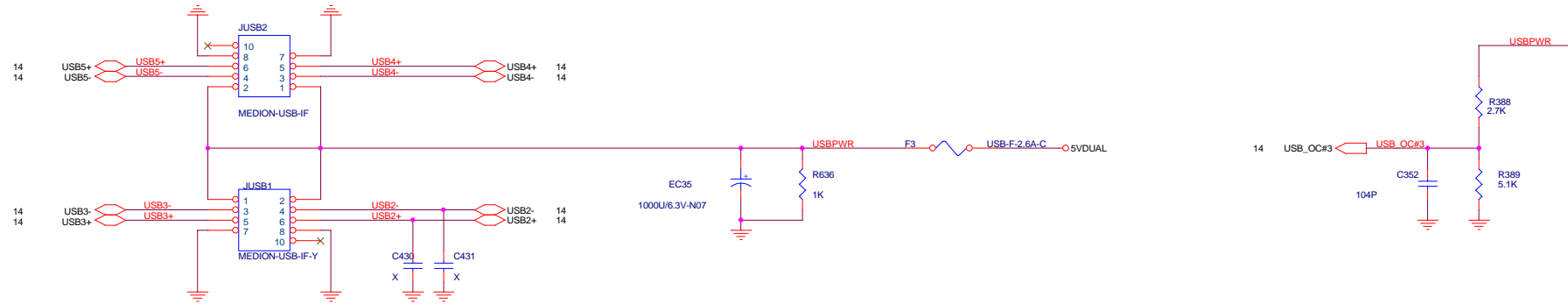
Micro Star Restricted Secret		
Title	MS-5 ACPI Controller	Rev 1.0
Document Number	MS-7048	
MICRO-STAR INT'L No. 65, Hsiao Pu St., Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, January 02, 2004 Sheet 21 of 28

Voltage Regular Module

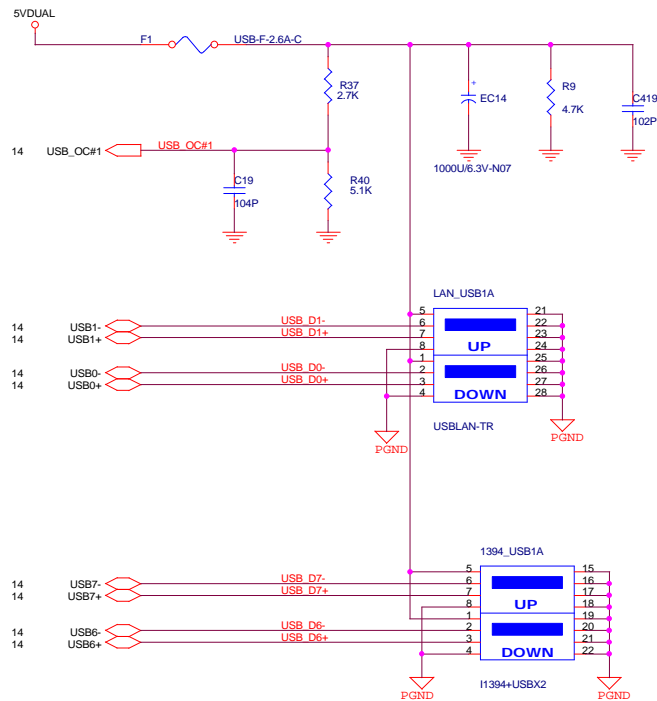
ATX12V Power Connector



FRONT USB PORT



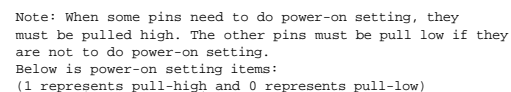
REAR USB PORT



- * USB Trace width : 7.5 mils
- * USB Trace Spacing : 20 mils
- * Differential USB Signlas Trace, Spacing : 7.5 mils

Micro Star Restricted Secret		
Title	Front USB Port	Rev
Document Number	MS-7048	1.0
MICRO-STAR INT'L No. 66, Sec. 2, St. Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Sunday, December 28, 2003
Sheet		23 of 28

LPC SUPER I/O W83637HF



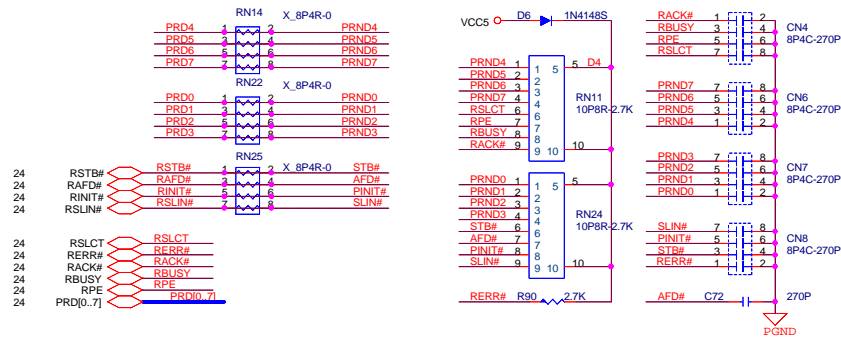
	0	1	
RTSA#	2E	4E	I/O CONFIGURATION
DTRA#	DEFAULT	ALL 0	I/O PORT BASE
SOUTA	KBC DISABLE	KBC ENABLE	KBC HARDWARE S/W
SOUTB	CLK 24M	CLK 48M	PIN18 INPUT CLK

SPEAKER BLOCK

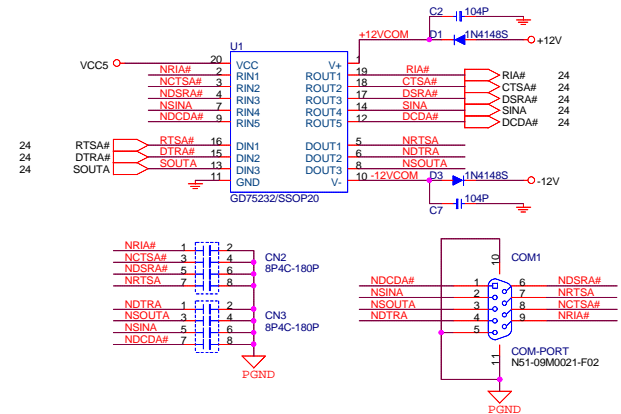


LPT/COM Port/FAN

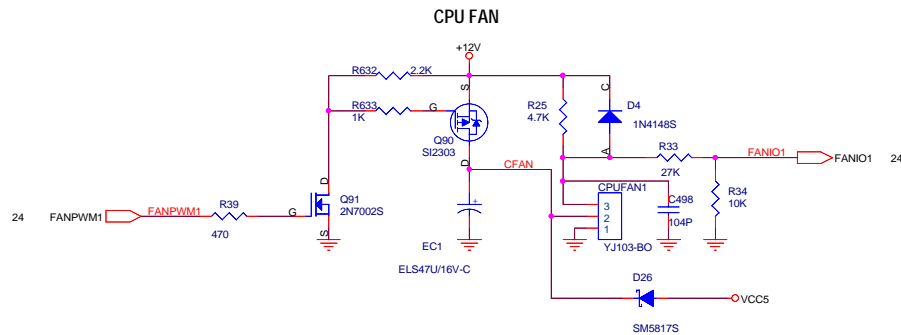
PARALLAL PORT



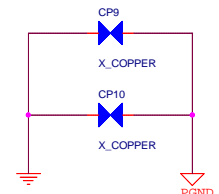
SERIAL PORT 1



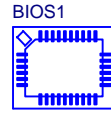
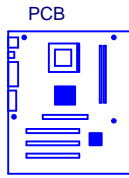
SMART FAN



EMI

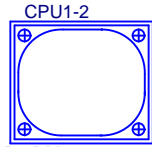
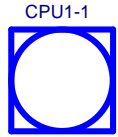


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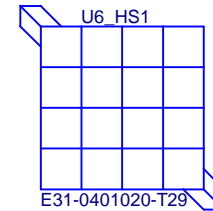
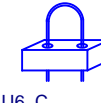
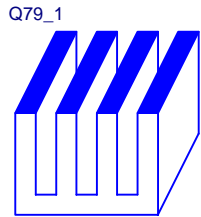


JAUDIO1(1-2),(3-4)

- X_YJUMPER-MG JAUD1(5-6)
- X_YJUMPER-MG JAUD1(9-10)
- YJUMPER-MG JBAT1(1-2)



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